CLAIMS

What is claimed is:

1. An RFID circuit for use within an RFID tag, the circuit including:

first clock generation circuitry to generate a modulator clock signal within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second clock generation circuitry to generate a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag.

2. The circuit of claim 1, wherein the second clock generation circuitry includes a second oscillator, and wherein the second clock generation circuitry is to recover a clock signal from the radio-frequency signal received at the RFID tag, to compare the recovered clock signal to an oscillator clock signal generated by the second oscillator of the RFID circuit, and to store a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID circuit.

3. The circuit of claim 2, wherein the second clock generation circuitry includes calibration circuitry to calibrate the second oscillator of the RFID circuit utilizing the second calibration value.

4. The circuit of claim 2, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

5. The circuit of claim 1, wherein the first clock generation circuitry includes a first oscillator, and is to retrieve the first calibration value from the non-volatile memory associated with the RFID tag, and to generate the modulator clock signal by calibrating in the first oscillator utilizing the first calibration value.

6. The circuit of claim 1, wherein the first clock generation circuitry is to generate a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

7. A method of generating a demodulator clock signal and a modulator clock signal within an RFID circuit for use within an RFID tag, the method including:

generating a modulator clock signal utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag;

generating the demodulator clock signal from a radio-frequency signal received at the RFID tag.

8. The method of claim 7, wherein the generating of the demodulator clock signal includes recovering a clock signal from the radio-frequency signal received at the RFID tag, comparing the recovered clock signal to an oscillator clock signal generated by a second oscillator of the RFID circuit, and storing a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID tag.

9. The method of 8, wherein the generating of the demodulator clock signal includes

calibrating the second oscillator of the RFID circuit utilizing the second calibration value.

10. The method of claim 8, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

11. The method of claim 7, including retrieving the first calibration value from the non-volatile memory associated with the RFID tag, wherein the generating of the modulator clock signal includes calibrating a first oscillator of the RFID circuit utilizing the first calibration value.

12. The method of claim 7, including generating a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

13. An RFID circuit for use within an RFID tag, the circuit including:

first means for generating a modulator clock signal within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second means for generating a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag.

14. A machine-readable medium storing a description of an RFID circuit for use in an RFID tag, said RFID circuit comprising:

first clock generation circuitry to generate a modulator clock signal within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second clock generation circuitry to generate a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag.

15. The machine-readable medium of claim 14, wherein the description comprises a behavioral level description of the circuit.

16. The machine-readable medium of claim 15, wherein the behavioral level description is compatible with a VHDL format.

17. The machine-readable medium of claim 15, wherein the behavioral level description is compatible with a Verilog format.

18. The machine-readable medium of claim 14, wherein the description comprises a register transfer level netlist.

19. The machine-readable medium of claim 14, wherein the description comprises a transistor level netlist.